CLAIMS:

1. A process of communicating to test access ports within an integrated circuit using a first protocol compliant with IEEE 1149.1 and second protocol different from IEEE 1149.1 comprising the steps of;

communicating to said test access ports using said first protocol to setup communication to the test access ports using said second protocol, and thereafter;

communicating to said test access ports using said second protocol.

2. A process of testing circuitry coupled to a test access port within an integrated circuit, said test access port having an interface operable to communicate in a first mode using IEEE 1149.1 protocol and in a second mode using a protocol different from said IEEE 1149.1 protocol comprising the steps of;

communicating to the test access port interface using said first mode to setup for testing said circuitry using said second mode, and thereafter

communicating to said test access port interface using said second mode to test said circuitry.

3. A process of accessing circuitry coupled to a test access port within an integrated circuit, said test access port having an interface operable to communicate in a first mode using IEEE 1149.1 protocol and in a second mode using a protocol different from said IEEE 1149.1 protocol comprising the steps of;

communicating to the test access port interface using said first mode to setup for accessing said circuitry using said second mode, and thereafter

communicating to said test access port interface using said second mode to access said circuitry.

4. A process of switching a test access port from responding to 1149.1 protocol to responding to another protocol comprising the steps of;

shifting an instruction into an instruction register of said test access port using said 1149.1 protocol,

updating the instruction from said instruction register using said 1149.1 protocol, and;

enabling, in response to said updating, the test access port to respond to said another protocol.

5. A process of testing a plurality of intellectual property core circuits within an integrated circuit comprising the steps of;

loading test instructions into two or more of said core circuits using a first test interface,

enabling a first group of one or more said core circuits to execute their respective test instructions in response to said first test interface, and;

enabling a second group of one or more said plurality of core circuits to execute their respective test instructions in response to a second test interface that is separate from the first test interface.

6. A process of accessing a scan data register within an integrated circuit, comprising the steps of,

selecting a first access protocol,

accessing the scan data register using said first access protocol,

selecting a second access protocol, and

accessing the scan data register using said second access protocol.

7. The process of claim 6 wherein the scan data register is an internal scan register.

8. The process of claim 6 wherein the scan data register is an in-circuit emulation register.

9. The process of claim 6 wherein the scan data register is an in-circuit programming register.

10. The process of claim 6 wherein the scan data register is a boundary scan register.

11. The process of claim 6 wherein the scan data register is a bypass register.

12. An integrated circuit comprising at least one dual mode test access port.

13. An integrated circuit comprising;

a set of data registers, and

a dual mode test access port for providing access to said set of data registers.

14. An integrated circuit comprising;

one or more intellectual property cores, each one or more intellectual property cores including a dual mode test access port, and

an externally accessible scan path connected to said dual mode test access port of each of said one or more intellectual property cores.

15. A circuit for selectively disabling and enabling an 1149.1 TAP comprising;

a first input for receiving an 1149.1 TAP disable signal,

a second input for receiving an 1149.1 TAP enable signal, and

an output operable in a first mode to disable the 1149.1 TAP in response to receiving said disable signal and in a second mode to enable the 1149.1 TAP in response to receiving said enable signal.

16. A test architecture within an integrated circuit, comprising;

an 1149.1 TAP test interface;

an alternate test interface,

a set of data registers accessible from one of said TAP and alternate test interfaces, and;

a test interface selection circuit, for selecting one of said TAP and alternate test interfaces for accessing said set of data registers.